C. Amendments to the Claims.

1. (Currently Amended) A semiconductor device, comprising:

a trench element separation region including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating separate semiconductor elements;

an oxide film formed on inner walls of the trench;

a trench filling insulating material filling the trench and having edges above the inner walls of the trench that are defined by **direct contact with** side edges of a sacrificial layer formed by a pullback etching process including a neutral radical that is performed for the trench filling process; and

wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane when viewed in cross section.

2. (Cancelled) The semiconductor device of claim 1, wherein the edges of the trench filling insulating material are defined by side edges of a sacrificial layer.

3. (Previously Amended) The semiconductor device of claim 1, wherein the sacrificial layer is a silicon nitride film.

4. (Cancelled) The semiconductor device of claim 3, wherein:

the side edges of the sacrificial layer are formed by an etching process including a neutral radical.

5. (Original) The semiconductor device of claim 1, wherein the semiconductor elements are insulated gate field effect transistors (IGFETs).

6. (Original) The semiconductor device of claim 5, wherein the IGFETs include opposite conductivity types.

7. (Previously Amended) A semiconductor device, comprising:

a trench element separation region including a trench formed in a surface of a semiconductor substrate, the trench element separation region isolating a first doped channel layer of a first insulated gate field effect transistor (IGFET) from a second doped channel layer of a second IGFET;

an oxide film formed on inner walls of the trench;

a trench filling insulating material filling the trench and having edges above the inner walls of the trench defined by **direct contact with** side edges of a sacrificial layer formed by a pullback etching process including a neutral radical performed before filling the trench; and

wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material are formed so as to be essentially located on the same plane when viewed in cross section.

8. (Cancelled) The semiconductor device of claim 7, wherein the edges of the trench filling insulating material are defined by side edges of a sacrificial layer.

9. (Previously Amended) The semiconductor device of claim 7, wherein:

the etching process includes a fluorine radical.

10. (Original) The semiconductor device of claim 7, wherein the first and second doped channel layers are of the same conductivity types.

11. (Original) The semiconductor device of claim 7, wherein the first and second doped channel layers are of opposite conductivity types.

12. (Withdrawn) A method for forming a trench element separation region on a surface of a semiconductor substrate, comprising the steps of:

depositing a first insulation film onto the surface of the semiconductor substrate;

depositing and patterning a second insulation film to form a second insulation film pattern;

dry etching the semiconductor substrate using the second insulation film pattern as an etching mask to form a trench;

forming an oxide film on an inner wall of the trench by thermally oxidizing the semiconductor substrate using the second insulation film pattern as an oxidation mask;

removing a modified layer formed on the surface of the second insulation film during the thermal oxidation step by using a neutral radical including fluorine;

etching the surface of the second insulation film by a predetermined thickness after the modified layer is removed;

depositing a filling insulation film over the whole surface of the trench to completely fill the trench after the surface of the second insulation film is etched; and

chemically mechanical polishing the filling insulation film using the second insulation film as a polishing stopper to form a trench filling insulating material.

13. (Withdrawn) The method for manufacturing a semiconductor device according to claim 12, wherein:

the second insulation film includes a silicon nitride film.

14. (Withdrawn) The method for manufacturing a semiconductor device according to claim 12, wherein:

the semiconductor substrate is a silicon substrate and the neutral radical is a fluorine radical.

15. (Withdrawn) The method for manufacturing a semiconductor device according to claim 14, wherein:

a final judgment of the modified layer removal is performed by measuring a change in intensity of emissions with a wavelength of approximately 336 nm from a reaction product NH.

16. (Withdrawn) The method for manufacturing a semiconductor device according to claim 14, wherein:

a final judgment of the modified layer removal is performed by measuring a change in intensity of emissions with a wavelength of approximately 388 nm from a reaction product CN.

17. (Withdrawn) The method for manufacturing a semiconductor device according to claim 14, wherein:

the thickness of the second insulation film is etched for adjustment such that edges of the trench insulating material above the inner walls of the trench are essentially located on the same plane as edges of the inner walls of the trench in a top section of the trench.

18. (Withdrawn) The method for manufacturing a semiconductor device according to claim 14, further including the step of:

forming a doped channel layer of an insulated gate field effect transistor (IGFET) by ion implantation and heat treatment after the trench filling insulating material is formed.

19. (Withdrawn) The method for manufacturing a semiconductor device according to claim 14, wherein:

the first insulation film is a silicon oxide film formed by thermal oxidation of the semiconductor substrate; and

the filling insulation film is a silicon oxide film deposited by a vapor deposition method.

20. (Withdrawn) The method for manufacturing a semiconductor device according to claim 14, wherein:

the trench element separation region isolates a first insulated gate field effect transistor (IGFET) from a second IGFET.

21. (New) The semiconductor device of claim 1, wherein:

above the surface of the substrate, the oxide film extends essentially only horizontally, is formed below and terminates beyond the edges of the trench filling insulating material above the inner walls.

22. (New) A semiconductor device isolation structure, comprising:

a trench formed in a semiconductor substrate;

a liner oxide film formed on the inner walls of the trench; and

a trench filling insulating material within the trench having

a liner oxide film defined edge within the trench, and

a neutral radical pullback etch defined edge above the trench that is aligned with the edges of the trench when viewed in cross section.

23. (New) The semiconductor device isolation structure of claim 22, wherein:

an insulated gate field effect transistor diffusion layer formed in the substrate adjacent to the trench.

24. (New) The semiconductor device isolation structure of claim 22, wherein:

the liner oxide film has a thickness greater than 7 nanometers.

25. (New) The semiconductor device isolation structure of claim 22, wherein:

the liner oxide film includes a substrate portion, the substrate portion extending essentially only horizontally on a surface of the semiconductor substrate, formed below and terminating beyond the neutral radical pullback etch defined edge.